ADDRESS WRAP FUNCTION FOR ADDRESSABLE MEMORY DEVICES

ABSTRACT

The invention is a selectable function that permits the address portion of data words to be separated from the storable content portion and that address portion to be used for different purposes without disturbing the stored contents in the memory array. The invention may be viewed as a command capability that permits analysis of signals for errors in such items as addresses, impedance calibration, timing, and component drift that develop in and between regions of an overall memory array.

Techniques are advanced involving data responsive selectable array circuitry modification for such operations as address correctness verification, machine timing and component drift correction purposes.

The principles are illustrated with memory systems built of Synchronous Dynamic Random Access Memory with Double Data Rate (SDRAM-DDR) elements.